Electronic Version
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# Claims

[c1] 1.A method for fabricating a trench capacitor of DRAM devices, comprising:
providing a semiconductor substrate having a pad oxide layer and a pad nitride layer formed thereon;
etching a deep trench into the pad nitride layer, the pad oxide layer and the semiconductor substrate;
doping the deep trench to form a buried doped plate in the semiconductor substrate adjacent to a lower portion of the deep trench, the buried doped plate serving as a first electrode of the trench capacitor;
forming a node dielectric layer on interior surface of the deep trench;
depositing a first conductive layer on the node dielectric layer inside the deep trench;
recessing the first conductive layer to a first depth in the deep trench, the first conductive layer serving as a second electrode of the trench capacitor;
depositing a spacer silicon layer on the node dielectric layer on sidewall of the deep trench;
locally ion doping an upper portion of the spacer silicon layer;
selectively removing the non-doped spacer silicon layer

to expose the node dielectric layer;

removing the exposed node dielectric layer to expose a silicon surface inside the deep trench, and simultaneously forming a dielectric spacer protecting the pad oxide layer; and

simultaneously oxidizing the exposed silicon surface inside the deep trench and the doped spacer silicon layer, thereby forming a thermal silicon oxide layer and an oxide spacer, respectively.

[c2] 2.The method of claim 1 wherein after oxidizing the exposed silicon surface inside the deep trench and the doped spacer silicon layer, the method further comprises:

forming a collar oxide layer on sidewall of the deep trench;

forming a second polysilicon layer atop the first polysilicon layer inside the deep trench;

recessing the second polysilicon layer to a second depth inside the deep trench;

wet etching the collar oxide layer that is not covered by the recessed second polysilicon layer;

removing the oxide spacer; and

removing the dielectric spacer.

[c3] 3.The method of claim 1 wherein the spacer silicon layer is made of amorphous silicon.

[c4] 4.The method of claim 1 wherein the spacer silicon layer has a thickness of about 100~150 angstsoms.

[c5] 5.The method of claim 1 wherein the method of locally ion doping an upper portion of the spacer silicon layer includes tilt angle ion implantation.

[c6] 6.The method of claim 1 wherein the method of locally ion doping an upper portion of the spacer silicon layer includes doping $BF_2$ ions.

[c7] 7.The method of claim 1 wherein the node dielectric layer is oxide-nitride-oxide (ONO) dielectric.

[c8] 8.The method of claim 1 wherein the node dielectric layer is oxide-nitride (ON) dielectric.

[c9] 9.The method of claim 1 wherein the node dielectric layer comprises silicon nitride.

[c10] 10.The method of claim 1 wherein the step of selectively removing the non-doped spacer silicon layer to expose the node dielectric layer involves the use of diluted ammonia solution.